2 of Stolt et al, data passes between the memory array and the microprocessors through the DP under the control of the DC. Data does not pass from the DC to the data port of the microprocessors. Thus, the DP has only one data port, i.e., the data port coupled to the memory array which is coupled to the data port of the microprocessor via the system bus.

Reference is made to Col. 4, beginning at line 36 of Stolt et al.:

> On the datapath side, shown in FIG. 2, the DP component of the MC supports the data flow between the system bus and the memory array and is disassociated from the memory control interfaces since al controls for the bus and the memory are generated by the DC components. The main functions of the DP component are to provide a 64 bit datapath from the bus to the memory, to provide ECC support for data both on the bus and in the memory, to scrub (or correct) any correctable errors in the memory array and to provide support for single clock cycle data transfer bursts.

Thus, Examiner's comment that the "data buffering section (e.g., fig. 2, buffers, DPU, IRQ, BED) adapted to couple data ***from one of a plurality of data ports*** to a data port of a microprocessor selectively in accordance with a control signal (e.g., figs 1-2, els. a microprocessor port (emphasis added) is not understood.

The Commissioner is hereby authorized to charge payment of any additional fees associated with this communication or credit any overpayment to Deposit Account No. 50-0845.

Respectfully submitted,

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Date

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